Amendments to and Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-14 (canceled)

Claim 15 (currently amended) A method of making an electronic module, comprising:

providing an integrated circuit, wherein the integrated circuit comprises a top face and a bottom face;

creating a multi-layer ~~redistributed~~ surface on [[a]] the top face of the integrated circuit, including:

creating a redistribution layer comprising at least a layer of conductive redistribution material above at least some portions of [[a]] the top face of the integrated circuit, which redistribution layer is electrically connected to the integrated circuit and includes conductive traces, mounting pads, and interconnect pads;

using at least some of the traces to position at least some of the interconnect pads along at least one edge of the multi-layer ~~redistributed~~ surface;

creating a layer of insulation above at least some portions of the redistribution layer;

mounting at least one secondary component to at least one mounting pad;

securing the bottom face of the integrated circuit to a substrate, which substrate includes electrical traces, wherein at least one trace terminates along at least one edge of the substrate; and

electrically connecting at least one interconnect pad along at least one edge of the multi-layer ~~redistributed~~ surface and at least one trace along at least one edge of the substrate, thereby electrically connecting the substrate to the integrated circuit.

Claim 16 (currently amended) The method of claim 15 further comprising electrically connecting additional components to at least the top face of the integrated circuit to form an electronics package of a microstimulator.

Claim 17 (currently amended) The method of claim 15 further comprising

providing a core comprising two separate halves;

securing one core half to the multi-layer ~~redistributed~~ surface of the integrated circuit;

securing one core half to a portion of the substrate; and

winding a wire around the core halves to create a coil assembly.

Claim 18 (original) The method of claim 17 wherein the core, when the two halves are assembled, is a dumbbell shape.

Claim 19 (original) The method of claim 15 wherein the at least one secondary component is at least one of a diode, a capacitor, a power source, and a coil.

Claim 20 (original) The method of claim 15 further comprising creating a first layer of insulation on at least some portions of the top face of the integrated circuit.

Claim 21 (currently amended) The method of claim 20 wherein creating the redistribution layer comprises:

creating a first layer of bond material on at least some portions of the top face of the integrated circuit;

creating a layer of conductive redistribution material on at least some portions of the first bond layer; and

creating a second layer of bond material on at least some portions of the redistribution material.

Claim 22 (currently amended) The method of claim 21 wherein the first bond layer covers portions of the top face of the integrated circuit and portions of the first insulation layer, and wherein the conductive redistribution material covers the first bond layer, and wherein the second bond layer covers the redistribution material.

Claim 23 (currently amended) The method of claim 21 wherein the multi-layer ~~redistributed~~ surface comprises at least one of copper, polyimide, gold, and titanium tungsten.

Claim 24 (original) The method of claim 20 further comprising:

creating a grounding layer comprising at least a layer of shielding material above at least some portions of the integrated circuit.

Claim 25 (original) The method of claim 24 wherein creating a grounding layer comprises:

creating a first layer of grounding bond material on at least some portions of the integrated circuit;

creating a layer of shielding material on at least some portions of the first grounding bond layer; and

creating a second layer of grounding bond material on at least some portions of the shielding material.

Claim 26 (currently amended) The method of claim 25 wherein the first layer of grounding bond material covers portions of the top face of the integrated circuit and portions of the first insulation layer, and wherein the layer of shielding material covers the first grounding bond layer, and wherein the second grounding bond layer covers the layer of shielding material.

Claim 27 (original) The method of claim 15 wherein at least a portion of the post-processing is performed on a wafer containing multiple integrated circuits.

Claims 28-32 (canceled)